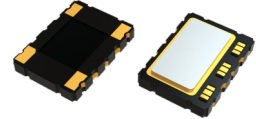


7.0x5.0mm SMD Voltage Controlled Temperature Compensated Crystal Oscillator

Feature

- Typical 7.0 x 5.0 x 1.9 mm SMD package
- Stratum 3 (Overall ± 4.6 ppm including 20 years aging)
- CMOS and Clipped Sine wave (without DC-cut capacitor) output optional



Electrical Specifications

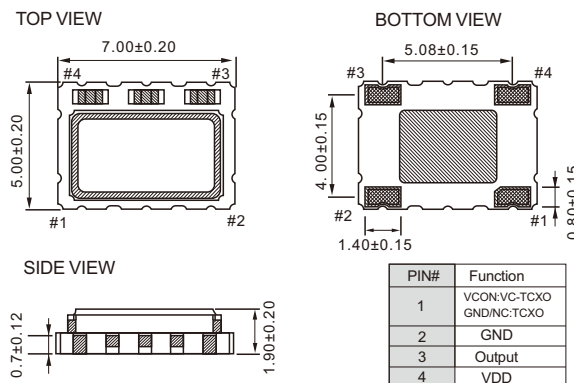
Parameter		5.0V		3.3V		Unit
		Min.	Max.	Min.	Max.	
Supply Voltage Variation		VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		5	52	5	52	MHz
Standard Frequency		10,12.8,16.384,19.2,19.44,20,25,26				MHz
Operating Temp. Range		-20~+70 / -40~+85				℃
Frequency stability (Overall, 20 Years)*		-	±4.6	-	±4.6	ppm
Frequency Stability Vs Temp. Range (Ref. to (FMAX+Fmin)/2)		-	±0.14 (-20~+70℃)	-	±0.14 (-20~+70℃)	ppm
		-	±0.28 (-40~+85℃)	-	±0.28 (-40~+85℃)	
Holdover Stability +		-	±0.32		±0.32	ppm
Supply Current	CMOS output	-	6	-	6	mA
	Clipped Sine Wave	-	3.5	-	3.5	
Output Level (CMOS)	Output High	90% VDD	-	90% VDD	-	V
	Output Low		10% VDD		10% VDD	
	Duty	45	55	45	55	%
Output Level (Clipped Sine Wave)		0.8	-	0.8	-	Vp-p
Load	CMOS	15pF		15pF		
	Clipped Sine Wave	10kΩ//10pF		10kΩ//10pF		
Control Voltage Range(VCTCXO)		0.5	2.5	0.5	2.5	V
Pulling Range (VCTCXO)		±5	-	±5	-	ppm
Vc Input Impedance(VCTCXO)		100	-	100	-	kΩ
Phase Noise @10.0MHz	100Hz	-130				dBc/Hz
	1KHz	-145				
	10KHz	-154				
Start Time		-	2	-	2	mSec
Storage Temp. Range		-55	125	-55	125	℃

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

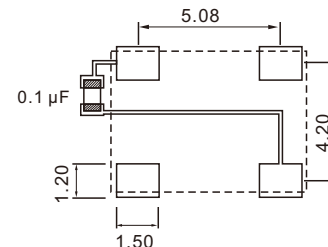
* Including calibration @ 25°C, supply voltage VDD $\pm 5\%$, load $\pm 10\%$, reflow soldering, 20 years aging and frequency stability over temperature.

+ Including 24hours aging, supply voltage VDD $\pm 5\%$ and frequency stability over temperature.

Dimension(mm)



Solder Pad Layout(mm)



To ensure optimal oscillator performance, place a by-pass capacitor of 0.1 μ F as close to the part as possible between Vdd and GND pads.