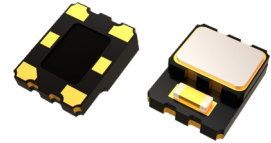


3.2x2.5mm High Frequency Temperature Compensated Crystal Oscillator

Feature

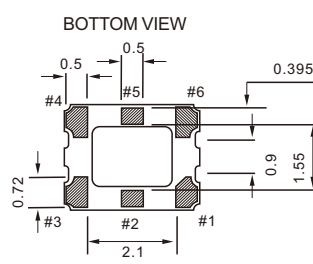
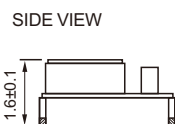
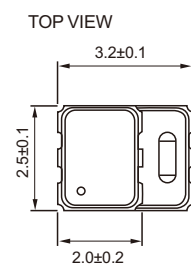
- Low power supply voltage: 3.3V and 2.5V options
- Clock output: CMOS, LVPECL, LVDS options
- CMOS output frequency support from 10MHz TO 250MHz
- Differential output frequency supports from 10MHz to 1.5GHz
- Low Phase Jitter typical 0.8 pS RMS at 12KHz to 20MHz frequency offsets
- Low current consumption, Pb-free/RoHS compliant
- Frequency Stability ± 2.0 ppm over -40°C to 85°C



Electrical Specifications

Parameter		LVPECL		LVDS		CMOS		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage		3.3V or 2.5V						V
Supply Voltage Variation		V _{DD} -5%	V _{DD} +5%	V _{DD} -5%	V _{DD} +5%	V _{DD} -5%	V _{DD} +5%	
Frequency Range		10	1500	10	1500	10	250	MHz
Supply Current		-	54	-	45	-	40	mA
Output Level	Output High	V _{DD} -1.03	V _{DD} -0.6	-	1.6	90%V _{DD}	-	V
	Output Low	V _{DD} -1.85	V _{DD} -1.6	0.9	-	-	10%V _{DD}	
Transition Time(Rise/ Fall Time)		-	0.5(20-80%)	-	1.0(20-80%)	-	3.0(20-80%)	nSec
Duty Cycle		45	55	45	55	45	55	%
Start time		-	5	-	5	-	5	mSec
Tri-State mode (input to pin 2)	Enable	70%V _{DD}	-	70%V _{DD}	-	70%V _{DD}	-	
	Disable	-	30%V _{DD}	-	30%V _{DD}	-	30%V _{DD}	
Stand by Current		-	20	-	20	-	20	mA
Output Loading		50 Ω into V _{DD} -2V		100 Ω		15pF		
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At V _{DD} =3.3V, F _{out} =250MHz	1kHz offset	-107	-	-107	-	-107	-	dBc/Hz
	10kHz offset	-111	-	-111	-	-111	-	
	100kHz offset	-114	-	-114	-	-114	-	
	1MHz offset	-125	-	-125	-	-125	-	
	20MHz offset	-147	-	-147	-	-147	-	
RMS Phase Jitter(12KHz to 20MHz)		0.8	1.5	0.8	1.5	0.8	1.5	pSec

Dimension(mm)



Type	CMOS	Differential
Pad	Function	Function
1	No Connection	No Connection
2	Tri-State	Tri-State
3	GND	
4	Output	Output
5	No Connection	Comp. Output
6	Supply Voltage(V _{DD})	

PIN Assignments

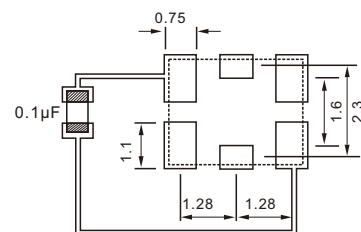
(LVPECL LVDS)

VDO	OUT-	OUT
6	5	4
1	2	3
NC	OE	GND

(CMOS)

VDO	NC	OUT
6	5	4
1	2	3
NC	OE	GND

Solder Pad Layout(mm)



To ensure optimal oscillator performance, place a by-pass capacitor of 0.1 μF as close to the part as possible between V_{DD} and GND pads.

FREQ. STABILITY vs. TEMP. RANGE

Temp. ($^{\circ}\text{C}$) \ ppm	± 1.0	± 2.0	± 2.5
-30 ~ +85	○	○	○
-40 ~ +85	△	○	○

Inclusive of calibration @ 25°C , operating temperature load variation, aging (1st year), shock, and vibration