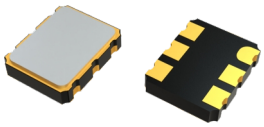
7.0 × 5.0 mm SMD LVPECL /LVDS Crystal Oscillator

Feature

- Typical 7.0 x 5.0 x 1.75 ceramic SMD package
- Very low phase jitter : < 1 ps (0.6ps, typ.) RMS
- Any frequency between 10 MHz and 1500 MHz
- Tri-state enable/disable
- Fast delivery



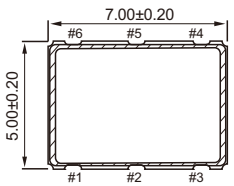
Electrical Specifications

Parameter		LVPECL				LVDS				Unit
		3.3V		2.5V		3.3V		2.5V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation		3.135	3.465	2.375	2.625	3.135	3.465	2.375	2.625	V
Frequency Range		10	1500	10	1500	10	1500	10	1500	MHz
Standard Frequency		106.25,125,133.33,150,155.52,156.25,187.5,212.5,312.5,622.08								MHz
Supply Current 10 MHz≦FO<1500MHz		-	50	-	50	-	50	-	50	mA
Output level	Output High	2.275	-	1.475	-	-	1.6	-	1.6	V
	Output Low	-	1.68	-	0.88	0.9	-	0.9	-	
Transition Time : Rise/Fall Time		-	1.0	-	1.0	-	1.0	-	1.0	nSec
Start Time		-	10	-	10	-	10	-	10	mSec
Tri-State (Input to Pin 1/2)	Enable	2.31	-	1.75	-	2.31	-	1.75	-	V
	Disable	-	0.99	-	0.75	-	0.99	-	0.75	
RMS Phase Jitter(integrated 12KHz ~ 20MHz)			1	-	1	-	1	-	1	pSec
Phase Noise @156.25MHz	100Hz	-94		-94		-94		-94		dBc/Hz
	1KHz	-113		-113		-113		-112		
	10KHz	-122		-122		-122		-122		
Aging(@25 1st year)		-	±3	-	±3	-	±3	-	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	-55	125	°C

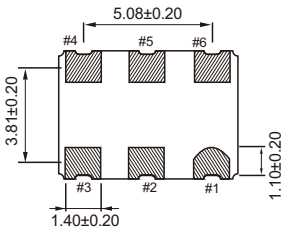
.+ Transition times are measured between 20% and 80% of VDD.

Dimension(mm)

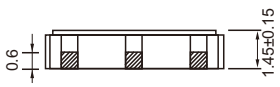
TOP VIEW



BOTTOM VIEW

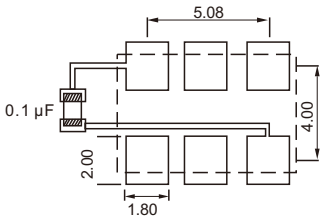


SIDE VIEW



PIN#	Function
1	NC/Tri-State
2	Tri-State/NC
3	GND
4	Output
5	Comp Output
6	VDD

Solder Pad Layout(mm)



To ensure optimal oscillator performance, place a by-pass capacitor of 0.1 μF as close to the part as possible between Vdd and GND pads.

FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C) \ ppm	±25	±50
-10 ~ +60	o	o
-20 ~ +70	o	o
-40 ~ +85	Δ	o

o: Available Δ:Conditional X: Not available
Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration